IN THE CLAIMS

The following is a complete listing of the claims:

1. (currently amended) A programmable interconnect circuit, comprising

a plurality of input/output (I/O) cells arranged into a plurality of N I/O blocks, wherein each I/O block includes at least two I/O cells and each I/O cell includes a multiplexer and a register associated with a pin of the programmable interconnect circuit; ~~and~~

a plurality of N routing structures corresponding to the plurality of N I/O blocks, each routing structure configured to receive signals from the plurality of I/O cells and programmable route the signals to each I/O cell within the routing structure's I/O block, wherein the register of each I/O cell comprises an output enable register coupled to the I/O block's routing structure, the output enable register controlling an output buffer coupling an output from the I/O cell's output register to its pin.

2. (cancelled)

3. (cancelled)

4. (currently amended) The programmable interconnect circuit of claim 1 ~~2~~, wherein the register of each I/O cell within a I/O block further comprises an input register coupled to the I/O block's routing structure and to the I/O cell's pin and further comprises an output register coupled to the I/O block's routing structure and to the I/O cell's pin, and wherein each multiplexer within each I/O cell is configured to select among a plurality of M signals programmably routed through the multiplexer's I/O cell's I/O block's routing structure to produce a multiplexer output signal, and wherein each I/O cell's output register is coupled to receive its I/O cell's multiplexer output signal.

5. (original) The programmable interconnect circuit of claim 4, wherein each I/O cell's multiplexer within a I/O block is a 4:1 multiplexer such that the plurality of M signals selected among by each 4:1 multiplexer comprises four signals.

LAW OFFICES OF
MACPHERSON KWOK CHEN
& HEID LLP

2402 MICHELSON DRIVE
SUITE 210
IRVINE, CA 92612
(949) 752-7040
FAX (949) 752-7049

PAGE 4/9 * RCVD AT 7/31/2006 10:05:33 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/3 * DNIS:2731811 * CSID:9497527049 * DURATION (mm-ss):02-34

6. (original) The programmable interconnect circuit of claim 1, wherein the routing structures are configured to programmable route signals according to configuration data stored in a non-volatile memory.

7. (original) The programmable interconnect circuit of claim 6, wherein the non-volatile memory is in-system programmable.

8. (original) The programmable interconnect circuit of claim 5, wherein the plurality of I/O cells are arranged in quadrants, the four signals being selected among by each 4:1 multiplexer each originating from an I/O cell within any quadrant.

9. (original) The programmable interconnect circuit of claim 8, wherein each I/O block includes 16 I/O cells, whereby the programmable interconnect circuit may be used for bus-switching applications.

10. (previously presented) A programmable interconnect circuit, comprising:

a plurality of input/output (I/O) blocks, each block including at least two I/O cells, each I/O cell including a multiplexer coupled to an I/O circuit, the multiplexers sharing a common set of control signal paths coupled to their select terminals but having different sets of data signal paths coupled to their input terminals; and

a plurality of routing structures corresponding to the plurality of I/O blocks, each routing structure for receiving input signals and routing them to the corresponding I/O block, each routing structure being programmable to provide control signals for the common set of control signal paths and data signals for the different sets of data signal paths.

11. (original) The programmable interconnect circuit of claim 10, wherein the number of I/O cells per block is at least four.

12. (original) The programmable interconnect circuit of claim 10, wherein the number of I/O cells per block is at least sixteen.

13. (cancelled).

LAW OFFICES OF
MACPHERSON KWOK CHEN
& HEID LLP

2402 MICHELSON DRIVE
SUITE 210
IRVINE, CA 92612
(949) 752-7040
FAX (949) 752-7049

PAGE 5/9 * RCVD AT 7/31/2006 10:05:33 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/3 * DNIS:2731811 * CSID:9497527049 * DURATION (mm-ss):02-34

14. (previously presented) The programmable interconnect circuit of claim 10, wherein the number of I/O cells per block is at least four.

15. (previously presented) The programmable interconnect circuit of claim 10, wherein each routing structure comprises a programmable switch matrix.

16. (previously presented) The programmable interconnect circuit of claim 10, wherein each routing structure is programmable to route an input signal received from an I/O cell onto any of the data signal paths coupled to the input terminals of a multiplexer.

17. (previously presented) The programmable interconnect circuit of claim 10 including a control array within each I/O block, each routing structure coupled through the control array to the common set of control signal paths for the multiplexers and to the I/O circuits.

18. (previously presented) The programmable interconnect circuit of claim 10, wherein each routing structure is programmable to provide multiple parallel data buses to the its corresponding I/O block, each data bus comprising a data signal path from each set of data signal paths for the multiplexers, each data bus selectable through the common set of control signal paths for the multiplexers.

19. (previously presented) The programmable interconnect circuit of claim 10, wherein each routing structure includes non-volatile memory for storing configuration data for programming the routing structure, the memory being in-system programmable.

20. (previously presented) The programmable interconnect circuit of claim 10, wherein each multiplexer has four input terminals and two select terminals.

21. (previously presented) The programmable interconnect circuit of claim 10, wherein an I/O circuit within an I/O block includes an input register and an output register, each coupled to the corresponding routing structure and to an I/O pin.

LAW OFFICES OF
MACPHERSON KWOK CHEN
& HEID LLP

2402 MICHELSON DRIVE
SUITE 210
IRVINE, CA 92612
(949) 752-7040
FAX (949) 752-7049

PAGE 6/9 * RCVD AT 7/31/2006 10:05:33 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/3 * DNIS:2731811 * CSID:9497527049 * DURATION (mm-ss):02-34

22. (original) The programmable interconnect circuit of claim 21, wherein the I/O circuit further includes an output enable register coupled to the corresponding routing structure and to an output buffer, the output buffer couple to the I/O pin.

23. (original) A programmable interconnect circuit, comprising

a plurality of input/output (I/O) blocks, each block including a control array and at least two I/O cells, each I/O cell including a multiplexer coupled to an I/O circuit, the multiplexers sharing a common set of control signal paths coupled to the control array and to their select terminals but having different sets of data signal paths coupled to their input terminals; and

a plurality of routing structures for receiving input signals and routing them to I/O blocks, each routing structure being coupled to a corresponding I/O block and programmable to provide control signals to the control array for controlling the multiplexers and to provide data signals for the different sets of data signal paths.

24. (previously presented) A programmable interconnect circuit, comprising:

a plurality of input/output (I/O) blocks, each block including at least two I/O cells, each I/O cell including a multiplexer whose output terminal is coupled to an I/O circuit, each I/O circuit including input, output, and output enable registers and an I/O pin, the multiplexers sharing a common set of control signal paths coupled to their select terminals but having different sets of data signal paths coupled to their input terminals; and

a plurality of routing structures corresponding to the plurality of I/O blocks, each routing structure for receiving input signals and routing them to the corresponding I/O block.

25. (cancelled)

26. (previously presented) The programmable interconnect circuit of claim 24 wherein each routing structure is programmable to provide control signals for the common set of control signal paths and data signals for the different sets of data signal paths.

LAW OFFICES OF
MACPHERSON KWOK CHEN
& HEID LLP

2402 MICHELSON DRIVE
SUITE 210
IRVINE, CA 92612
(949) 752-7040
FAX (949) 752-7049

27. (previously presented) The programmable interconnect circuit of claim 26 including a control array within each I/O block, the corresponding routing structure coupled through the

PAGE 7/9 * RCVD AT 7/31/2006 10:05:33 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/3 * DNIS:2731811 * CSID:9497527049 * DURATION (mm-ss):02-34

control array to the common set of control signal paths for the multiplexers and to the I/O circuits.

LAW OFFICES OF
MACPHERSON KWOK CHEN
& HEID LLP

2402 MICHELSON DRIVE
SUITE 210
IRVINE, CA 92612
(949) 752-7040
FAX (949) 752-7049

PAGE 8/9 * RCVD AT 7/31/2006 10:05:33 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/3 * DNIS:2731811 * CSID:9497527049 * DURATION (mm-ss):02-34